In the Claims:

Please amend claims 1-4, 11-13, 19 and 20. Please cancel claims 5, 9, 14 and 18. Please add new claim 29, 30. The claims are as follows:

1. (Currently Amended) A method ~~of forming an FinFET device~~, comprising:

~~(a) providing a semiconductor substrate;~~

[[(b)]]forming a dielectric layer on a top surface of [[said]] a semiconductor substrate;

forming a silicon layer on a top surface of said dielectric layer;

forming a patterned hardmask on a top surface of said silicon layer;

[[(c)]]removing said silicon layer where said silicon layer is not protected by said patterned hardmask thereby forming a silicon fin on a top surface of said dielectric layer;

removing said patterned hardmask and a less than whole portion of said dielectric layer from under said fin;

[[(d)]]forming a conformal protective layer on at least one sidewall of said fin, said protective layer extending under said fin; and

[[(e)]] removing said protective layer from said at least one sidewall and from under said fin in a channel region of said fin.

2. (Currently Amended) The method of claim 1, further including between ~~steps (d) and (e)~~ said forming said protective layer and said removing said protective layer, performing at least one ion implantation step into said fin.

3. (Currently Amended) The method of claim 1, further including:

[[(f)]]forming a gate dielectric on exposed surfaces of said fin in said channel region, said gate dielectric extending under said fin; and

[[(g)]]forming a conductive gate on said gate dielectric.

4. (Currently Amended) The method of claim 3, further including:

[[(h)]]after said forming said conductive gate, removing said protective layer from source/drain regions of said fin.

5. (Canceled)

6. (Original) The method of claim 1, wherein said protective layer comprises tetraethoxysilane oxide or silicon nitride.

7. (Original) The method of claim 1, wherein said protective layer is about 15 to 50 Å thick.

8. (Original) The method of claim 1, wherein said fin has a height of about 500 to 2000 Å and has a width of about 200 to 500 Å.

9. (Canceled)

10. (Original) The method of claim 1, wherein said fin comprises mono-crystalline silicon.

11. (Currently Amended) A method ~~of forming an FinFET device~~, comprising:

~~(a) providing a semiconductor substrate;~~

[[(b)]]forming a dielectric layer on a top surface of [[said]] a semiconductor substrate;

forming a silicon layer on a top surface of said dielectric layer;

forming a patterned hardmask on a top surface of said silicon layer;

[[(c)]] removing said silicon layer where said silicon layer is not protected by said patterned hardmask thereby forming a silicon fin having a top surface and sidewalls on a top surface of said dielectric layer; ~~and~~

removing said patterned hardmask and a less than whole portion of said dielectric layer from under said fin; and

[[(d)]]forming a protective spacer on ~~at least~~ a lower portion of at least one of said sidewalls, said protective spacer not extending to said top surface of said fin, said protective spacer extending under said silicon fin.

12. (Currently Amended) The method of claim 11, further including:

[[(e)]]after forming said protective spacer, performing at least one ion implantation step into said fin.

13. (Currently Amended) The method of claim 11, further including:

[[(e)]]forming a gate dielectric on exposed surfaces of said fin in at least a channel region of said fin and over said protective spacer; and

[[(f)]]forming a conductive gate on said gate dielectric.

14. (Canceled)

15. (Original) The method of claim 11, wherein said protective spacer comprises tetraethoxysilane oxide or silicon nitride.

16. (Original) The method of claim 11, wherein said protective spacer is about 15 to 50 Å thick.

17. (Original) The method of claim 11, wherein said fin has a height of about 500 to 2000 Å and has a width of about 200 to 500 Å.

18. (Canceled)

19. (Currently Amended) [[The]] A method ~~of claim 11, wherein step (c) comprises~~ comprising:

forming a dielectric layer on a top surface of a semiconductor substrate;

forming a mandrel on a top surface of said dielectric layer;

depositing a conformal silicon layer on a top surface and a sidewall of said mandrel and on surfaces of said dielectric layer not covered by said mandrel;

removing said conformal silicon layer from said top surface of said mandrel and said surfaces of said dielectric layer not covered by said mandrel thereby forming a silicon spacer on said sidewall of said mandrel, said silicon spacer having a top surface and an exposed sidewall;

forming a protective spacer on a lower portion of said exposed sidewall of said silicon spacer, said protective spacer not extending to said top surface of said silicon spacer; and

removing said mandrel.

20. (Currently Amended) The method of claim 19, further including after ~~the step of removing~~ forming said silicon spacer, performing a high temperature anneal of said conformal silicon layer.

21. (Original) The method of claim 11, wherein said fin comprises mono-crystalline silicon.

22. (Withdrawn) An FinFET device, comprising:

a semiconductor substrate,

a dielectric layer on a top surface of said substrate;

a silicon fin having sidewalls, said fin on a top surface of said dielectric layer; and

a protective spacer on at least a lower portion of at least one of said sidewalls.

23. (Withdrawn) The FinFET device of claim 22, wherein said fin includes a channel region and source/drain regions.

24. (Withdrawn) The FinFET device of claim 22, further including:

a gate dielectric on surfaces of said fin in said channel region of said fin; and

a conductive gate on said gate dielectric.

25. (Withdrawn) The FinFET device of claim 22, wherein said protective spacer comprises tetraethoxysilane oxide or silicon nitride.

26. (Withdrawn) The FinFET device of claim 22, wherein said protective spacer is about 15 to 50 Å thick.

27. (Withdrawn) The FinFET device of claim 22, wherein said fin has a height of about 500 to 2000 Å and has a width of about 200 to 500 Å.

28. (Withdrawn) The FinFET device of claim 22, wherein said silicon fin comprises mono-crystalline silicon.

29. (New) The method of claim 3, wherein said fin has a top surface and first and second opposing sidewalls and said gate dielectric is formed said top surface and both said first and second sidewalls of said fin in said channel region.

30. (New) The method of claim 29, wherein said conductive gate is formed on said gate dielectric over said top surface and both said first and second sidewalls of said fin in said channel region.